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| 10/759,479 | 01/16/2004 | Paul Edwin O'Connor | 200-66500 (PB040048AF) | 7577 |

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| EXAMINER | |
|---|---|
| HOUSHMAND, HOOMAN | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/759,479 | O'CONNOR ET AL. | |
| | Examiner | Art Unit | |
| | Hooman Houshmand | 2419 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 101*

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claim(s) 12-17, 18, 19, 20 is/are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to particular machine, or (2) transform underlying subject matter (such as an article or material) to a different state or thing. See page 10 of In Re Bilski 88 USPQ2d 1385. The instant claims are neither positively tied to a particular machine that accomplishes the claimed method steps nor transform underlying subject matter, and therefore do not qualify as a statutory process.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-11, 12-17, 18, 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. The limitation (claim 1 lines 3-9) "*an active input memory circuit that has a plurality of addresses, the plurality of addresses having an associated plurality of keys and forwarding information, the active input memory circuit receiving a plurality of cells, extracting key information from each cell, and comparing the key information from each cell with the keys, the active input memory circuit outputting forwarding information for a cell when the key information of the cell matches a key*" is indefinite. It is unclear what the antecedent basis for "the keys" is. The relationship between the various keys mentioned in the limitation is unclear. Furthermore the *active input memory circuit has a plurality of addresses*; it is unclear whether these *addresses* point out specific portions in the *memory circuit*.

6. The limitation (claim 1 lines 10-13) "*an active input routing circuit that is connected to the active input memory circuit, the active input routing circuit receiving the plurality of cells, and forwarding information from the active input memory circuit for a number of the cells*" is indefinite. There is a grammatical error. It is unclear if *forwarding information* to *the active input memory circuit,* or, receiving *forwarding information from the active input memory circuit* - was intended.

7. The limitation (claim 12 lines 1-3) "*a circuit that has a plurality of addresses that have an associated plurality of keys and forwarding information*" is indefinite. It is unclear what the relationship between the *circuit* and the *addresses* is. It is unclear what is meant by *a circuit* having *a plurality of addresses*.

8. The limitation (claim 18 lines 1-3) "*a circuit that has a plurality of addresses that have an associated plurality of keys, forwarding information, control/data flags, and*

*enable/disable flags*" is indefinite. It is unclear what this *circuit* is. It is unclear what is meant by *a circuit* having *a plurality of addresses*.

9. The limitation (claim 19 lines 7-9, 10-12) "*writing a plurality of data routes with valid routing information to the first local controller; addressing the second local controller over the bus, and writing a plurality of data routes with valid routing information to the second local controller*" is indefinite. It is expected that *routing information* needs to be valid.

## *Claim Rejections - 35 USC § 102*

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Noven (US 5809501 A).

**Claim 12**. Noven teaches (3:33-4:18 24-bit or 28-bit global address of an ATM cell, connection database stored in each local exchange. When an ATM cell arrives at an ATM exchange port, it causes a lookup request to be sent to the connection database along with the global address values as parameters. When the connection database receives a lookup request with these parameters, it determines the local address corresponding to the global address values received. The global address of an ATM cell is first mapped to a local address that is specific to an ATM exchange port, a search algorithm is then used to look up entries in the database) *a method of operating a circuit that has a plurality of addresses that have an associated plurality of keys and*

*forwarding information, the method comprising the steps of: receiving a plurality of cells; extracting key information from each cell; comparing the key information from each cell with the keys, and outputting forwarding information for an input cell when the key information of the input cell matches a key* (6:66-7:6 FIG. 3, switching and cross-connection of virtual channels and virtual paths within an ATM link. VP switching refers to the switching of an ATM cell using only the upper part of the identifier field, the field VPI; in VP/VC switching the entire identifier field, both the VPI and the VCI, are used to switch an ATM cell).

### ***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noven, in view of Sanchez (US 20040090970 A1).

**Claim 1**. Noven teaches (3:33-4:18 24-bit or 28-bit global address of an ATM cell, connection database stored in each local exchange. When an ATM cell arrives at an ATM exchange port, it causes a lookup request to be sent to the connection database along with the global address values as parameters. When the connection database receives a lookup request with these parameters, it determines the local address

corresponding to the global address values received. The global address of an ATM cell is first mapped to a local address that is specific to an ATM exchange port, a search algorithm is then used to look up entries in the database) *a communication system comprising: an active input circuit having: an active input memory circuit that has a plurality of addresses, the plurality of addresses having an associated plurality of keys and forwarding information, the active input memory circuit receiving a plurality of cells, extracting key information from each cell, and comparing the key information from each cell with the keys, the active input memory circuit outputting forwarding information for a cell when the key information of the cell matches a key; and an active input routing circuit that is connected to the active input memory circuit, the active input routing circuit receiving the plurality of cells, and forwarding information from the active input memory circuit for a number of the cells, the active input routing circuit transmitting an input cell in response to forwarding information for the input cell* (6:66-7:6 FIG. 3, switching and cross-connection of virtual channels and virtual paths within an ATM link. VP switching refers to the switching of an ATM cell using only the upper part of the identifier field, the field VPI; in VP/VC switching the entire identifier field, both the VPI and the VCI, are used to switch an ATM cell).

Noven does not teach *transmitting a cell onto a bus*.

In the same field of endeavor, Sanchez discloses ([0054] logic 111 and processor 105 are located at different locations, and bus 109 includes a communication

link between the two locations implemented via a virtual circuit over the link) *transmitting a cell onto a bus*.

It would have been obvious, to a person having ordinary skill in the art at the time that the invention was made, to combine the teachings of Sanchez with Noven to complete the communication link between the two locations.

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noven, in view of Terrell (US 7292567 B2).

**Claim 18**. Noven teaches (3:33-4:18 24-bit or 28-bit global address of an ATM cell, connection database stored in each local exchange. When an ATM cell arrives at an ATM exchange port, it causes a lookup request to be sent to the connection database along with the global address values as parameters. When the connection database receives a lookup request with these parameters, it determines the local address corresponding to the global address values received. The global address of an ATM cell is first mapped to a local address that is specific to an ATM exchange port, a search algorithm is then used to look up entries in the database) *a method of operating a circuit that has a plurality of addresses that have an associated plurality of keys, forwarding information*.

Noven does not teach *control/data flags, and enable/disable flags, setting the enabled/disabled flags to enabled for each address unless the address has a key that matches a predetermined pattern*.

In the same field of endeavor, Terrell discloses (53:48-54:31 A method for revising the configuration of a plurality of routing processors includes in any order: for each virtual entity and each routing processor to be reconfigured, each processor that uses routing information implementing routing for a particular virtual entity, setting a flag to indicate that routing for the virtual entity is disabled; routing to a managing processor for disposition subsequently received frames, both control frames and data frames that indicate the virtual entity as a destination; enabling proxy processes performed by the managing processor to respond to or route such subsequent frames; storing new routing information for a virtual entity in a memory accessible by a routing processor; and clearing the flags in routers previously set so as to enable routing of traffic for the virtual entity in accordance with the new routing information. New routing information may be stored in one router, for access by one or more routing processors or frame processors or in several routers facilitating routing for one or more virtual entities, for distributing the processing burden of virtualization, security, or redundancy) *control/data flags, and enable/disable flags, setting the enabled/disabled flags to enabled for each address unless the address has a key that matches a predetermined pattern*.

It would have been obvious to a person having ordinary skill in the art, at the time that the invention was made, to combine the teachings of Terrell with Noven, thus modifying Noven to include control/data flags, and enable/disable flags, setting the

enabled/disabled flags to enabled for each address unless the address has a key that matches a predetermined pattern – to develop an architecture for differentiated services.

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klinker (US 20060182034 A1), in view of Miyagi (US 5661722 A).

**Claim 19**. Klinker discloses ([0296] FIG. 26 data structure 2610, routing table, repository, database, or any of a number of other data structures. Data structure 2610 may be used to store data and other information for use by flow control system 200 FIG. 2. Data such as IP addresses, prefix/netmask, latency, next hop in information, next hop out information, convergence point identification, user configurable operating parameters stored in data structure 2610. Data gathered in response to path trace and active probing used. Using recorded information such as IP addresses or conditions recorded in data structure 2610 enables the creation of a topological network map, from which data routes are constructed. Candidate path convergence point IP addresses are stored in data structure 2610 for topologically-mapping network data routes. Aggregating IP addresses of convergence points between a source and a destination node or point enables efficient data route control) *a method of operating a controller connected to first and second local controllers via a bus, the method comprising the steps of: addressing the first local controller over the bus and writing a plurality of control routes to the first local controller; addressing the second local controller over the*

*bus and writing a plurality of control routes to the second local controller; addressing the first local controller over the bus, and writing a plurality of data routes with valid routing information to the first local controller; addressing the second local controller over the bus, and writing a plurality of data routes with valid routing information to the second local controller; addressing the first local controller over the bus and writing an enable all command to the first local controller; and addressing the second local controller over the bus and writing an enable control command to the second local controller*.

Klinker does not disclose *a circuit connected to a controller*.

In the same field of endeavor, Miyagi teaches (2:54-58 performance monitoring cell checking circuit and the performance monitoring cell generation circuit, which are connected to a controller in an exchange, receive an instruction for checking the first user cell stream and generating the second performance monitoring cell stream) discloses *a circuit connected to a controller*.

It would have been obvious to a person having ordinary skill in the art, at the time that the invention was made, to combine the teachings of Miyagi with Klinker, thus modifying Klinker to explicitly include a circuit connected to a controller, to perform usage parameter control.

15. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mathewes (US 4669081 A), in view of Miyagi.

**Claim 20**. Mathewes teaches (4:6-30 FIG. 1 the BIT maintenance controller BMC 12 sets up a serial test vector word and appends the fault parameter word of the fault to be examined at the end of the test vector word transmission. After transmitting the test vector word, the BMC 12 disables the test mode and generates a single system clock to determine the response to this stimulus. An LSD chain 24 response to the system clock and fault insertion is determined by the BMC 12 shifting out an LSD chain word from the integrated circuit 10 and at the same time shifting in a new test vector or returning the IC 10 to its original logic condition. During some operational tests a fault may be left inserted while system testing proceeds. The BMC 12 interfaces with both the fault word register 14 and the timing and control 17 of the IC 10. The timing and control 17 receives shift enable/ and LSD clock/ timing signals from the BMC 12. The shift enable/ signal in conjunction with the LSD clock/ causes the generation of timing signals to shift the serial LSD input 11 from the BIT maintenance controller 12 into the integrated circuit 10) *a method comprising the steps of: detecting a failure condition; when a failure condition has been detected, outputting a disable data command to the first local controller; and outputting an enable all command to the second local controller*.

Mathewes does not disclose *a circuit connected to a controller*.

In the same field of endeavor, Miyagi teaches (2:54-58 performance monitoring cell checking circuit and the performance monitoring cell generation circuit, which are connected to a controller in an exchange, receive an instruction for checking the first

user cell stream and generating the second performance monitoring cell stream) discloses *a circuit connected to a controller*.

It would have been obvious to a person having ordinary skill in the art, at the time that the invention was made, to combine the teachings of Miyagi with Mathewes, thus modifying Mathewes to explicitly include a circuit connected to a controller, to perform parameter control.

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hooman Houshmand whose telephone number is (571) 270-1817. The examiner can normally be reached on Monday - Friday 8am - 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. H./
Examiner, Art Unit 2419

/Jayanti K. Patel/
Supervisory Patent Examiner, Art Unit 2419